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Nenand Rijavec	
Appln. No.: 10/065,745	Art Unit: 2625
Filed: November 14, 2002	Examiner: Peter K. Huntsinger
For: APPARATUS, METHOD AND PROGRAM PRODUCT FOR CONTROLLING PRINTING	

Mail Stop **APPEAL BRIEF – PATENTS**
Commissioner for Patents
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APPEAL BRIEF UNDER 37 CFR §41.37(a)

Appellants have filed a timely Notice of Appeal from the final Office action, dated May 18, 2007. A single copy of this brief is provided pursuant to 37 C.F.R. §41.37(a). An authorization to charge the appropriate fee is included herewith. Please charge any deficiencies in fees and credit any overpayment of fees to IBM Corporation Deposit Account No. 50-3669 and advise us accordingly.

I. Real Party in Interest:

International Business Machines Corporation is the real party in interest in the above referenced patent application.

II. Related Appeals and Interferences:

The appellant is aware of no other appeals or interferences that will directly affect or have a bearing on this appeal.

III. Status of The Claims:

Claims 1 – 11 are currently pending.

Claims 1 – 11 are currently rejected.

Claims 1 – 11 are the subject of this appeal and are appended hereto in the "Claims Appendix" attached hereto.

No claims have been withdrawn, cancelled or allowed.

IV. Status of Amendments:

All prior amendments have been entered.

V. Summary of The Claimed Subject Matter:

Independent Claim 1

The invention, as recited by claim 1, is an apparatus that includes a pipeline 10, of elements 21, 22a – n, 25, 24a – h, processing print control data. *See, e.g.*, paragraphs

0023 – 31 of the application with reference to Figure 2, a copy of which is included as Exhibits A in the Evidence Appendix of this Appeal Brief. More particularly, the pipeline 10 includes multiple print head drivers 24a – h, raster image processor (RIP) machines 22a – n and a sequencer 21. The input port of the sequencer 21 receives a print data stream. Paragraph 0023 ("The first stage is a sequencer 21 which receives a data stream from a print server."). The sequencer 21 monitors data flows among the pipelined elements and parses the print data stream into local data portions related to individual pages and global state data portions related to characteristics shared across multiple pages. Paragraph 0024. The sequencer 21 packages together parsed page local and global state data portions. *Id.* The output port of the sequencer 21 is networked and communicates with, and is directly connected to, the input ports of the RIP machines 22a – n. Paragraph 0026 ("The Page RIP pipeline stage 22 contains, in the illustrated form, a number of separate RIP machines 22a, 22b, 22c . . . 22n. To minimize the network contention, these machines may be connected to the sequencer 21 using multiple physical networks.") – Paragraph 0028. Each RIP machine 22a – n receives parsed page data. Paragraph 0027 ("Each time a RIP machine can accept another work unit, it contacts the sequencer 21 and obtains the next unit of work. Depending on the size and speed of the RIP machines, each may be working on multiple work units."). The RIP machines 22a – n process in parallel packaged parsed page data and generate data signals for the print head drivers 24a – h as directed by the sequencer 21. Paragraph 0033 ("The local portions are then passed to a plurality of RIP machines and processed in parallel in a plurality of raster image processing machines at 101 to produce print head data streams appropriate to drive the print heads of an associated printer, here described as being bitmap data streams."). Each RIP machine 22a – n output port communicates 25 with the input port of the print head drivers 24a – h to deliver data signals to control the application of colorant to a sheet. Paragraph 0029 ("the RIP-to-head driver communication may be split into multiple networks, shown in FIG. 2 at 25 as being interposed between the RIP machines 22a et seq and the head drivers 24a et seq.").

Dependent claim 10 recites that the result of the connection of the sequencer 21 output port to the input ports of the RIP machines 22a – n is, that the sequencer 21 remains unchanged by additions and removals of RIP machines 22a – n. *See, e.g.*, Figure 2 and Paragraph 0010 ("By using the design described here, each controller can be configured, by adding RIP machines and connecting networks, to suit the needs of each customer.").

Independent Claim 5

The invention, as recited by claim 5, is an apparatus that includes a pipeline 10, of elements 21, 22a – n, 25, 24a – h, connected between a print server 11 and a printer 12 and processing print control data from the print server 11. *See, e.g.*, the above description of claim 1 with regard to pipeline 10 and, paragraphs 0020 – 31 of the application with reference to Figure 1, a copy of which is included as Exhibits B in the Evidence Appendix of this Appeal Brief. In addition to reciting the pipeline of claim 1 connected between a print server 11 and a printer 12, claim 5 recites that the raster image processors convert data from a form communicated as a print data stream into a variable number of bit maps that depend upon whether an individual page is to be blank, printed with a single color or printed with multiple colors. Paragraph 0028 ("As each work unit is RIPed, a number of bitmaps are produced. The number can be either zero (blank page), 1 (single color), 4 (CMYK) or even more if the print engine uses more than four colors.").

Dependent claim 11 recites that the sequencer output port is connected to the input ports of the raster image processors', which may be connected and disconnected without changing the sequencer. *See, e.g.*, Figure 2 and Paragraph 0010 ("By using the design described here, each controller can be configured, by adding RIP machines and connecting networks, to suit the needs of each customer.").

Independent Claim 6

The invention, as recited by claim 9, is a method of that may be practiced by the apparatus (i.e., the pipeline 10) of claim 1 in the apparatus of claim 5 (i.e., a printer including the pipeline 10). *See, e.g.*, paragraph 0033 of the application with reference to Figure 3, a copy of which is included as Exhibit C in the Evidence Appendix of this Appeal Brief. The method begins in step 100 by receiving a print data stream from a print server and parsing the stream into local and global portions. Paragraph 0033. Global print stream data portions are packaged together with parsed local print stream data portions. Paragraph 0024. The packaged print stream data portions may be queued, if needed. Paragraph 0025. In step 101 queued packages are communicated directly over a network to the RIP machines. *Id* ("This queue is accessed by the Page RIP processors in the next pipeline stage."). The RIP machines process packages to generate print head driving data signals. Paragraph 0028. Finally, in step 102 the generated print head driving data signals are communicated to a printer and to the print heads of said printer. *Id* ("The RIP machine reports that the unit was done to the sequencer and then sends the bitmaps to the next pipeline stage, the head drivers 24a et seq.").

Independent Claim 9

The invention, as recited by claim 9, is a computer program product on a computer readable medium 200 with program instructions stored thereon and effective when executed by a computer system to cause the computer system to practice the method of claim 6. *See, e.g.*, paragraph 0034 of the application with reference to Figure 4, a copy of which is included as Exhibit D in the Evidence Appendix of this Appeal Brief.

VI. Grounds of Rejection to Be Reviewed on Appeal:

1. Claim 9 is finally rejected under 35 USC §101.

2. Claims 10 and 11 are finally rejected under 35 USC §112.

3. Claims 1 and 3 are finally rejected under 35 USC §103(a) as being unpatentable over U.S. Patent No. 6,825,943 to Barry et al. in view of U.S. Patent No. 6,315,390 to Fujii et al.

4. Claims 2 and 6 – 11 are finally rejected under 35 USC §103(a) as being unpatentable over Barry et al. and Fujii et al. in further view of U.S. Patent No. 6,532,016 to Venkateswar et al.

5. Claims 4 and 5 are finally rejected under 35 USC §103(a) as being unpatentable over Barry et al. and Fujii et al. in further view of U.S. Patent No. 5,946,460 to Hohensee et al.

VII. Argument:

REJECTION OF CLAIM 9 UNDER 35 U.S.C. §101

Claim 9 recites a "computer program **product** comprising a **computer readable medium** with program **instructions stored thereon** and effective when executed by a computer system to cause the computer system[1]" and, therefore, claim 9 is statutory.

"[A] claimed computer-readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and is thus statutory.[2]" "While the mere **use** of the machine **to collect** data necessary for application of the **mental process** may not make the claim patentable subject matter, see In re Grams, 888 F.2d 835, 839-840 (Fed. Cir. 1989), these claims in **combining the use** of machines with a mental process, claim patentable subject matter.[3]"

The *sole basis* for rejecting claim 9 as directed to non-statutory subject matter asserted in the Final Office action (Final), mailed May 18, 2007, is that, "[c]laim 9 is directed to a computer program. For claim 9 to be statutory, the appellant must state 'A computer readable medium storing a computer program' (or equivalent) not a computer program comprising a computer readable medium." Appellants previously noted that claim 9 already recited "computer program **product** comprising a **computer readable medium** with program **instructions stored thereon**[4]" in an Amendment After Final (AAF), filed July 19, 2007. The Advisory Action (Advisory), mailed July 24, 2007, asserted that "Based on the appellant's specification, the computer program product can

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[1] Lines 1 – 3 (emphasis added).
[2] See *Lowry*, 32 F.3d at 1583-84, 32 USPQ2d at 1035.
[3] *In re* Comiskey, Case No. 2006-1286, at page 23 – 24 (Fed. Cir., September 20, 2007).
[4] *Supra* (emphasis added).

be data signals embodied in a carrier wave. Therefore, regardless of whether the product comprises a computer-readable medium, the appellant is claiming a computer program.[5]"

Appellant is unaware of any basis, statutory, administrative or in the black letter law, that stands for the proposition that: "computer readable medium storing a computer program" is statutory; but a "computer program **product** comprising a **computer readable medium** with program **instructions stored thereon** and effective when executed by a computer system to cause the computer system" is not. This is totally arbitrary. Furthermore, there is no way, of which the appellant is aware, that computer program instructions could be stored on a "carrier wave" as alleged in the Advisory. Nor has anything been made of record to show how anything could be stored on a "carrier wave." Absent such a showing, the rejection cannot be sustained.

Therefore, claim 9 recites statutory subject matter under 35 U.S.C. §101 and the final rejection must be reversed.

REJECTION OF CLAIMS 10 AND 11 UNDER 35 U.S.C. §112

Claims 10 and 11 are enabled by the application as filed because a skilled artisan would understand that as a result of networking the sequencer 21 with the RIP machines 22a – n, that the sequencer 21 remains unchanged by adding and removing RIP machines 22a – n.

"The test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in

[5] Page 3, third paragraph.

the art without undue experimentation.[6]" A patent need not teach, and preferably omits, what is well known in the art[7].

As recited by the present application, "each controller can be configured, by adding RIP machines and connecting networks, to suit the needs of each customer.[8]" So, the system may be customized based on user needs, adding (or removing) RIP machines to suit the user. Further, "[t]he sequencer maintains a queue of the independent work units that were generated in this way. This queue is accessed by the Page RIP processors in the next pipeline stage.[9]" So, the sequencer divides print jobs into smaller units, but the RIP machines themselves decide which unit to take and when to take it. "To minimize the network contention, these machines may be connected to the sequencer 21 using multiple physical networks.[10]" Clearly the network(s) is(are) analogous to Ethernet with the RIP machines operating independently and in parallel. Moreover,

> Each time a RIP machine can accept another work unit, **it contacts** the sequencer 21 **and obtains** the next unit of work. Depending on the size and speed of the RIP machines, each may be working on multiple work units. Note also that the RIP machines can be of varying sizes and may be significantly different than the sequencer. For example, the sequencer 21 may be a high end machine with excellent I/O performance, while the RIP machines 22a et seq may be much cheaper and slower. Also note that this design, where each RIP machine requests more work when ready, provides for automatic load balancing.[11]

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[6] *United States v. Telectronics, Inc.,* 857 F.2d 778, 785, 8 USPQ2d 1217, 1223 (Fed. Cir. 1988)).
[7] *In re Buchner*, 929 F.2d 660, 661, 18 USPQ2d 1331, 1332 (Fed. Cir. 1991); *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 1384, 231 USPQ 81, 94 (Fed. Cir. 1986), *cert. denied*, 480 U.S. 947 (1987); and *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1463, 221 USPQ 481, 489 (Fed. Cir. 1984).
[8] Application as filed, page 3, lines 14 – 15.
[9] Paragraph 0025.
[10] Paragraph 0026.
[11] Paragraph 0026.

So, the sequencer and RIP machines are described in this example as networked independent computers[12]. When one adds a RIP machine, the added machine joins in contacting the sequencer 21 and obtaining next work units; when one is removed, the others take up the slack. This is transparent to the sequencer 21.

Therefore, claims 10 and 11 are enabled[13] by the application as filed and the final rejection must be reversed.

REJECTION UNDER 35 U.S.C. §103(a)

Neither Barry et al., Fujii, nor any other reference of record teaches or suggests "a sequencer which has an **output port** networked and communicating with, **and directly connected to**, the **input ports** of said plurality of raster image processors[14]… ." "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the **references**."[15]

CLAIMS 1 and 3 over Barry et al. and Fujii et al.

The Final asserts that Barry et al. discloses the "sequencer ([by] instruction operator for job file 114 of Fig. 1a) which has an output port which communicates with

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[12] See also, paragraph 0009 ("Instead of custom hardware and expensive fast multiprocessor machines, the controller is designed to use cheap commodity processors such as commercial, off the shelf, personal computer systems.").
[13] Certainly, if claims had been added that recited that connecting and disconnecting raster image processors changed the sequencer changed the sequencer, those claims would have been rejected as not being enabled and contrary to Fig. 2.
[14] Claim 1, lines 9 – 11 (emphasis added); see also, claims 5, 6 and 9.
[15] *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985) (emphasis added).

the input ports of said plurality of raster image processors (col. 4, lines 34-40)[16]" in Fig 1b. Copies of Barry et al. Figs 1a and 1b are included as Exhibits E and F, respectively, in the Evidence Appendix of this Appeal Brief. The Final relies upon Fujii et al. to "disclose a plurality of print head drivers, … (col. 6, lines 60-65)."

"Instruction operator 114 has an output along a line 116 to a distributor 118 in FIG. 1b.[17]" Thus, Barry et al. teaches an instruction operator 114 that is connected to a "distributor block 118 [that] is provided to distribute in multiple print job files, each multiple thereof having a select portion of the print job which was segmented or partitioned by instruction operator 114 for processing according to separate processes in a plurality of parallel sections of the print system illustrated in FIGS. 1a and 1b.[18]" So, the output of the Barry et al. instruction operator 114 is connected to a single Barry et al. functional unit, i.e., distributor 118. The Barry et al. "distributor 118 provides the print job file 104 including a first select portion 140 along a line 142 to a first RIP engine 150.[19]" Therefore, because Barry et al. requires this intervening distributor 118, the Barry et al. instruction operator 114 is not networked with the RIP engines and certainly not connected to the RIP engine inputs.

Furthermore, the Barry et al. distributor 118 has a fixed number of outputs; therefore it can only handle a fixed number of output paths.

> Distributor 118 has several other outputs including an output for a print job file having a second select portion 144 which is coupled along path 146 from distributor 118 to a second RIP engine 152. Similarly a print job file having an nth select portion 148 is also coupled from distributor 118 along a path 151 to an nth RIP engine 154 representing the last partitioned print job file having a select portion of the print job to be separately processed **in a parallel path**.[20]

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[16] Page 6, #6, second paragraph.
[17] Barry et al. col. 3, lines 22 – 23.
[18] Col. 5, lines 8 – 14.
[19] *Id*, lines 14 – 16.
[20] *Id*, lines 31 – 38 (emphasis added).

The output of the Barry et al. instruction operator 114 (which the Final alleges corresponds to the sequencer) is connected to distributor 118. It is not "directly connected to, the input ports of said plurality of raster image processors" as claim 1 recites. Further, Barry et al. specifically includes separate paths 142, 146 and 151 from the distributor 118 to the RIP engines 142. Adding another parallel path to Barry et al. for another (n+1st) RIP engine requires adding another output to the Barry et al. distributor 118.

The present application describes a number of drawbacks with prior art high speed printers with specificity[21]. Implicit in that description is that the present invention is directed to those drawbacks. Thus,

> it is a purpose of this invention to propose a radically different design for a high speed print controller. Instead of custom hardware and expensive fast multiprocessor machines, the controller is designed to use cheap commodity processors such as commercial, off the shelf, personal computer systems. Traditionally, such an approach has not been considered viable, since the commodity machines lacked high enough I/O and memory performance to be useful. This invention proposes to avoid this problem by introducing page pipelining, so that rasterized bitmaps are not returned to a common point. In this way, processing requirements on each part of the system are drastically lessened.
> As a result, a print controller has **much higher performance** and **lower cost** than currently feasible. In addition, as commodity processors and commercially available networks are improved, the performance can be increased in a straightforward manner. By using the design described here, each **controller** can be **configured**, by **adding RIP machines and connecting networks**, to suit the needs of each customer[22].

So with reference to Figure 2, because the sequencer 21 is networked to the Rip machines 22a – 22n in one ore more physical networks[23]; the number of connected Rip machines 22a – 22n can be changed without changing the sequencer 21 itself. Thus, if someone, e.g., a customer, decides more Rip machines 22a – 22n would improve performance,

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[21] Paragraphs 0002 – 8.
[22] Paragraphs 0009 – 10 (emphasis added).
[23] *Supra*.

more can be added[24] without changing the sequencer 21, simply by attaching more to the network(s). It follows that, likewise, if the customer, decides that some Rip machines 22a – 22n are unused or underused; they may be removed, e.g., to save power, without changing the sequencer 21, simply by detaching from the network. Neither Barry et al., nor any other reference of record, teaches or suggests this.

Further with regard to Fujii et al., the Final relies on col. 6, lines 60-65, which is directed to Fujii et al. Figure 3. A copy of Fujii et al. Figure 3 is included as Exhibit G in the Evidence Appendix of this Appeal Brief. Fujii et al. Figure 3 is a block diagram showing the control circuit 30 of a printer. The control circuit 30 includes a line inkjet head 35 with a head driver 34 driving an ink jet head 5. In particular, the Fujii et al. head driver 34 has application to a low cost commodity printer such as shown in Fujii et al. Figure 11, a copy of which is included as Exhibit H in the Evidence Appendix of this Appeal Brief. However, adding the Fujii et al. head driver 34 to Barry et al. (or more likely adding Barry et al. to Fujii et al.) does not change the fact the neither reference shows recites "a sequencer which has an **output port** networked and communicating with, **and directly connected to**, the **input ports** of said plurality of raster image processors[25]" as claim 1 recites. Therefore, the combination of Barry et al. with Fujii et al. fails to result in the present invention as recited in claim 1.

Accordingly, *prima facie* obviousness has not been established for claim 1 under 35 U.S.C. §103(a) over the combination of Barry et al. with Fujii et al. Since claims 2, 3 and 4 depend from claim 1, *prima facie* obviousness has not been established under 35 U.S.C. §103(a) for claim 3 over the combination of Barry et al. with Fujii et al. for the reasons set forth with respect to claim 1 or, for claim 2, 4 or any other claim depending from claim 1.

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[24] *Supra*.
[25] *Supra*.

CLAIMS 6 – 11 over Barry et al., Fujii et al. and Venkateswar et al.

Claims 10 and 11

Venkateswar et al. in combination with Barry et al. and Fujii et al. as described for claims 1 and 3 fails to result in the present invention as recited in claims 10 and 11 because one could not connect and disconnect raster image processors from the combination without changing the sequencer[26].

The Final asserts that Venkateswar et al. "discloses a sequencer (main processor 52) being connected to raster image processors (parallel processors 54) (Fig. 2a).)" A copy of Venkateswar et al. Fig 2a is included as Exhibit I in the Evidence Appendix of this Appeal Brief. Venkateswar et al. FIG. 2a shows a single-chip multiprocessor[27] with the master processor on the same chip as the parallel processors. Both the Venkateswar et al. master processor 52 and the parallel processors 54 are part of the same chip. One could not add and subtract processors from such a single chip.

Moreover, to read the Barry et al. instruction operator 114, distributor 118 and portion selectors 140, 144, 148 connected to the down stream RIP engines 150, 152, 154 to be a network; the combination must be considered a star configuration with distributor 118 as a central hub. Such a star configuration has dedicated connections, in this example, between the hub/distributor 118 (connected to what is alleged to be the sequencer, i.e., the upstream instruction operator 114) and portion selectors 140, 144, 148 connected to the down stream RIP engines 150, 152, 154. Adding another RIP engine to Barry et al., for example, requires adding another line/path.

[26] Claims 10 and 11, lines 3 – 5.
[27] "One embodiment of a sort-first implementation using a **single-chip multiprocessor** is shown in FIG. 2a." col. 5, lines 45 – 46 (emphasis added).

Even if one were to accept *arguendo* that the Venkateswar et al. main processor 52 were a sequencer within the meaning of the present application, the combination of the Barry et al. star distributor 116 with the Venkateswar et al. main processor 52 does not, without more, change the star configuration. Nor does it change the star configuration so that "the sequencer's said output port is connected to the raster image processors' said input ports, and wherein said raster image processors may be connected and disconnected to said sequencer output port, said sequencer remaining unchanged by additions and removals of connected and disconnected said raster image processors.[28]"

Therefore, Venkateswar et al. in combination with Barry et al. and Fujii et al. fails to result in the present invention as recited in claims 10 and 11 and *prima facie* obviousness has not been established for claims 10 and 11.

Claims 6 – 9

Independent claims 6 and 9 recite "communicating queued packaged print stream data portions **directly** to a plurality of raster image processors[29]," which is quite different than the combination of Barry et al. and Fujii et al., as set forth hereinabove. Nor is this shown by Venkateswar et al., or any other reference of record; nor is it asserted to be shown by Venkateswar et al. Therefore, the combination of Barry et al. with Fujii et al. and Venkateswar et al., alone or with any other reference of record, does not result in the present invention as recited in claim 6 or 9 or in claim 7 or 8, which depend from claim 6.

The Final relies on Barry et al. as described for claims 1 and 3 and turns to "Venkateswar et al. [to] disclose communicating queued packaged print stream data portions directly over a network (col. 2, lines 21-28).[30]" The Advisory asserts that

[28] Claims 10 and 11.
[29] Claim 6, lines 5 – 6; claim 9, 8 – 9 (emphasis added).
[30] Page 12, first full sentence.

"[a]ccording to the definition within the art, a network consists of a system or group of interconnected elements."

First, nothing is provided to indicate the source of this "definition." Second, given this definition, what doesn't qualify as a network? A system or group of disconnected elements? "During patent examination, the pending claims must be 'given their broadest **reasonable** interpretation **consistent with the specification**.'"[31]." Moreover, that "broadest reasonable interpretation of the claims **must also be consistent** with the interpretation that those skilled in the art would reach.[32]" The present application discusses this networked arrangement at numerous locations[33] and illustrates it in Figure 2.

In addition, Venkateswar et al. describes using dynamic scheduling for higher processor utilization[34]. This "uses a virtual buffer system. In this type of system, the first set of regions are assigned a like number of PEs. When a PE is done with its region, it picks up the next region in the pipeline.[35]" So, Venkateswar et al. specifically provides that a

> page is logically divided into several bands. **Suppose memory is available for the entire page**, then in the preferred embodiment the p parallel processors (PPs) **are first assigned** to the first p bands, where p is the number of PPs. As soon as a PP finishes generation of pixels for that band **it is assigned** to the next band to be processed in the sequence. After all the bands are rasterized, the frame buffer is transferred to the print engine for printing.[36]

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[31] *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000) ((emphasis added)).
[32] *In re Cortright*, 165 F.3d 1353, 1359, 49 USPQ2d 1464, 1468 (Fed. Cir. 1999).
[33] Paragraphs 0010, 17, 18, 26, 29 and 34.
[34] col. 4, lines 21 – 22.
[35] *Id*, lines 17 – 21.
[36] *Id*, lines 26 – 33 (emphasis added).

This is more or less represented in the upper portion of Venkateswar et al. Figure 2a with the MP storing output in chip memory and pushing tasks into the task queue[37]. In the second, lower portion of Figure 2a the MP schedules the PPs. So, a "scheduler process running on the MP operates in the following manner. A free band buffer and **PP are assigned** for each band in sequence. A server process running on the PP is allowed to rasterize the corresponding primitives for that band into the band buffer.[38]"

Nowhere in any of this is there anything about "communicating queued packaged print stream data portions directly over a network.[39]" Therefore, asserting that the Venkateswar et al. master processor 52 is networked with the Boundary Processing Rasterization in the Venkateswar et al. parallel processors 54 is inconsistent with both Venkateswar et al. and the present specification.

Therefore also, Venkateswar et al. in combination with Barry et al. and Fujii et al. fails to result in the present invention as recited in claims 6 and 9, as well as claims 7 and 8, which depend from claim 6 and *prima facie* obviousness has not been established for claims 6 – 9.

CLAIM 5 over Barry et al., Fujii et al. and Hohensee et al.

Nowhere has anything been provided in any Office action to show or suggest "a pipeline of elements connected **between** a print server and a printer and processing print control data from said print server,[40]" and wherein the pipeline elements are as claimed. Therefore, the combination of Barry et al. with Fujii et al. and Hohensee et al., alone or with any other reference of record, does not result in the present invention as recited in claim 5.

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[37] Col. 5, lines 45 – 60.
[38] Col. 4, lines 33 – 48 (emphasis added).
[39] *Supra*.
[40] Claim 5, lines 2 – 3 (emphasis added).

Without providing any substantive support for the allegation that the pipeline elements are connected between the printer server and printer, the Final asserts that:

> Barry et al. disclose[s] an apparatus comprising: a pipeline of elements connected between a printer server and a printer and processing print control data from said print server, and said pipeline of elements having: a plurality of raster image processors, each of which has an input port receiving parsed page data (Rip engines 150, 152, and 154 of Fig. 1b, col. 1, lines 41-50);[41] … .

The Final continues, relying on Fujii et al. solely to "disclose a plurality of print head drivers," and Hohensee et al. to "disclose each of said raster image processors converts data from a form communicated as a print data stream into a variable number of portions depending upon whether an individual page is to be blank or to be printed with a single color or to be printed with multiple colors (col. 4, lines 53-60)." Since the appellants have previously raised this, the Final asserts that "Barry et al. disclose a print head driver between a server and a printer (print driver 102 of Fig 1a, col. 3, lines 13 – 15).[42]"

Fujii et al. teaches with reference to Figure 2a that a "drive voltage pulse signal is applied by **head driver** 62 between the common electrode 61 and individual electrode 60 of the nozzle to be driven.[43]" A copy of Fujii et al. Figure 2a is included as Exhibit J in the Evidence Appendix of this Appeal Brief. Further, a "drive voltage pulse is applied appropriately from a head driver 34 to the corresponding ink jet head unit 5 to discharge an ink drop from the ink nozzle.[44]" By contrast, Barry et al. teaches that "[t]he print job input 100 is provided to a print driver 102 as a print job file 104 and is output from print driver 102 along a line 106 to a print spooler 108.[45]" Very clearly, the Barry et al. print driver 102 is not deriving a print head; and so, is not a print head driver within the plain meaning in the art as evidenced by Fujii et al. or within the meaning set forth in the

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[41] Page 10, #9.
[42] page 4, (g).
[43] Col. 6, lines 14 – 17 (emphasis added).
[44] Id, lines 67 – 69.
[45] col. 3, lines 13 – 15.

specification[46]. Nor does is this shown or suggested by Fujii et al., Hohensee et al. or any other reference of record.

Therefore the combination of Barry et al. with Fujii et al. and Hohensee et al. or further in combination with any reference of record, does not result in the present invention as recited in claim 5. Accordingly, since the combination of Barry et al. with Fujii et al. and Hohensee et al. does not result in the present invention as recited in claims 5, claim 5 is not made obvious under 35 U.S.C. §103(a) by Barry et al. with Fujii et al. and Hohensee et al. or further in combination with any reference of record.

Patentability of Claims 2 and 4 under 35 USC §103

Moreover, "If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious.[47]" Therefore, Barry et al. with Fujii et al. alone or further in combination with any reference of record, does not result in the present invention as recited by claims 2 and 4, which depend from claim 1.

Accordingly, since Barry et al. in combination with Fujii et al., alone or in further combination with any other reference of record, does not result in the present invention as recited in claims 1 – 11; *prima facie* obviousness under 35 U.S.C. §103(a) has not been shown for any of finally rejected claims 1 – 11 and the final rejection must be reversed.

CONCLUSION

Claim 9 recites a "computer program **product** comprising a **computer readable medium** with program **instructions stored thereon** and effective when executed by a computer system to cause the computer system[48]" and, therefore, claim 9 is statutory. Claims 10 and 11 are enabled by the application as filed because a skilled artisan would

[46] *Supra.*
[47] *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).
[48] Lines 1 – 3 (emphasis added).

understand that as a result the sequencer remains unchanged by adding and removing RIP machines. Neither Barry et al., Fujii, nor any other reference of record teaches or suggests "a sequencer which has an **output port** networked and communicating with, **and directly connected to**, the **input ports** of said plurality of raster image processors[49];" Venkateswar et al. in combination with Barry et al. and Fujii et al. fails to result in the present invention because one could not connect and disconnect raster image processors from the combination without changing the sequencer[50]; neither of Barry et al., Fujii et al., Venkateswar et al., or any other reference of record teaches "communicating queued packaged print stream data portions **directly** to a plurality of raster image processors[51];" No reference of record shows or suggests "a pipeline of elements connected **between** a print server and a printer and processing print control data from said print server,[52]" for the pipeline elements are as claimed.

Therefore, Barry et al. in combination with Fujii et al., alone or in further combination with any other reference of record, does not result in the present invention as recited in any of claims 1 – 11; *prima facie* obviousness under 35 U.S.C. §103(a) has not been shown for any of finally rejected claims 1 – 11; and, the final rejection must be reversed.

Respectfully submitted,

January 28, 2008
(Date)

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[49] *Supra*.
[50] Claims 10 and 11, lines 3 – 5.
[51] Claim 6, lines 5 – 6; claim 9, 8 – 9 (emphasis added).
[52] Claim 5, lines 2 – 3 (emphasis added).

CLAIMS APPENDIX

A copy of the claims involved in the appeal is provided below.

1. An apparatus comprising:

a pipeline of elements processing print control data and having:

a plurality of print head drivers, each of which controls the application of colorant to a sheet and has an input port receiving data signals;

a plurality of raster image processors, each of which has an output port communicating with the input ports of said plurality of print head drivers to deliver thereto data signals controlling the application of colorant to a sheet and an input port receiving parsed page data; and

a sequencer which has an output port networked and communicating with, and directly connected to, the input ports of said plurality of raster image processors and an input port receiving a print data stream, said sequencer monitoring data flows among the pipelined elements and parsing a print data stream into local data portions related to individual pages and global state data portions related to characteristics shared across a plurality of pages, said sequencer packaging together parsed page local and global state data portions;

said raster image processors processing in parallel packaged parsed page data related to a plurality of pages and generating data signals to be communicated to said print head drivers as directed by said sequencer.

2. An apparatus according to Claim 1 wherein said sequencer queues packaged individual page data to be communicated to said raster image processors and further wherein individual ones of said raster image processors draw from said queued data as processing of data related to an individual page is completed and generated data signals are communicated to a print head driver.

3. An apparatus according to Claim 1 wherein each of said raster image processors converts data from a form communicated as a print data stream to a form to be communicated as data signals to a print head driver.

4. An apparatus according to Claim 3 wherein each of said raster image processors converts data from a form communicated as a print data stream into a variable number of portions depending upon whether an individual page is to be blank or to be printed with a single color or to be printed with multiple colors.

5. An apparatus comprising:

a pipeline of elements connected between a print server and a printer and processing print control data from said print server, and said pipeline of elements having:

a plurality of print head drivers, each of which controls the application of colorant to a sheet and has an input port receiving data signals;

a plurality of raster image processors, each of which has an output port communicating with the input ports of said plurality of print head drivers to deliver thereto data signals controlling the application of colorant to a sheet and an input port receiving parsed page data; and

a sequencer which has an output port networked and communicating with the input ports of said plurality of raster image processors and an input port receiving a print data stream, said sequencer monitoring data flows among the pipelined elements and parsing a print data stream into local data portions related to individual pages and global state data portions related to characteristics shared across a plurality of pages, said sequencer packaging together parsed page local and global state data portions;

said plurality of raster image processors processing packaged parsed page data related to a plurality of pages in parallel and generating data signals to be communicated to said print head drivers as directed by said sequencer, each of said raster image processors converting data from a form communicated as a print

data stream into a variable number of bit maps depending upon whether an individual page is to be blank or to be printed with a single color or to be printed with multiple colors.

6. A method comprising the steps of:

receiving a print data stream from a print server and parsing the stream into local and global portions;

packaging together parsed local and global print stream data portions;

queuing packaged print stream data portions;

communicating queued packaged print stream data portions directly over a network to a plurality of raster image processors;

processing a plurality of communicated packaged print stream data portions in parallel to generate print head driving data signals; and

communicating the generated print head driving data signals to a printer and to the print heads of said printer.

7. A method according to Claim 6 wherein said step of packaging print stream data portions comprises packaging portions applicable to individual pages.

8. A method according to Claim 6 wherein said step of processing comprises generating bit map data signals.

9. A computer program product comprising a computer readable medium with program instructions stored thereon and effective when executed by a computer system to cause the computer system to:

receive a print data stream from a print server and parse the stream into local and global portions;

package together parsed local and global print stream data portions;

queue packaged print stream data portions;

communicate queued packaged print stream data portions directly to a plurality of raster image processors;

process a plurality of communicated packaged print stream data portions in parallel to generate print head driving data signals; and

communicate the generated print head driving data signals to a printer and to the print heads of said printer.

10. An apparatus as in claim 1, wherein the sequencer's said output port is connected to the raster image processors' said input ports, and wherein said raster image processors may be connected and disconnected to said sequencer output port, said sequencer remaining unchanged by additions and removals of connected and disconnected said raster image processors.

11. An apparatus as in claim 5, wherein the sequencer's said output port is connected to the raster image processors' said input ports, and wherein said raster image processors may be connected and disconnected to said sequencer output port, said sequencer remaining unchanged by additions and removals of connected and disconnected said raster image processors.

EVIDENCE APPENDIX

This section lists evidence submitted pursuant to 35 U.S.C. §§1.130, 1.131, or 1.132, or any other evidence entered by the Examiner and relied upon by Appellant in this appeal, and provides for each piece of evidence a brief statement setting forth where in the record that evidence was entered by the Examiner. Copies of each piece of evidence are provided as required by 35 U.S.C. §41.37(c)(ix).

Exhibit	EVIDENCE	BRIEF STATEMENT SETTING FORTH WHERE IN THE RECORD THE EVIDENCE WAS ENTERED BY THE EXAMINER
A	**Application Figure 1**	**Originally filed application and with the application filed November 14, 2002**
B	**Application Figure 2**	**Originally filed application and with the application filed November 14, 2002**
C	**Application Figure 3**	**Originally filed application and with the application filed November 14, 2002**
D	**Application Figure 4**	**Originally filed application and with the application filed November 14, 2002**
E	**Barry et al. Figure 1A**	**Cited in the first Office action mailed August 22, 2005**
F	**Barry et al. Figure 1B**	**Cited in the first Office action mailed August 22, 2005**
G	**Fujii et al. Figure 3**	**Cited in the first Office action mailed August 22, 2005**
H	**Fujii et al. Figure 11**	**Cited in the first Office action mailed August 22, 2005**
I	**Venkateswar et al. Figure 2A**	**Cited in the first Office action mailed August 22, 2005**
J	**Fujii et al. Figure 2a**	**Cited in the first Office action mailed August 22, 2005**
K		

EXHIBIT A

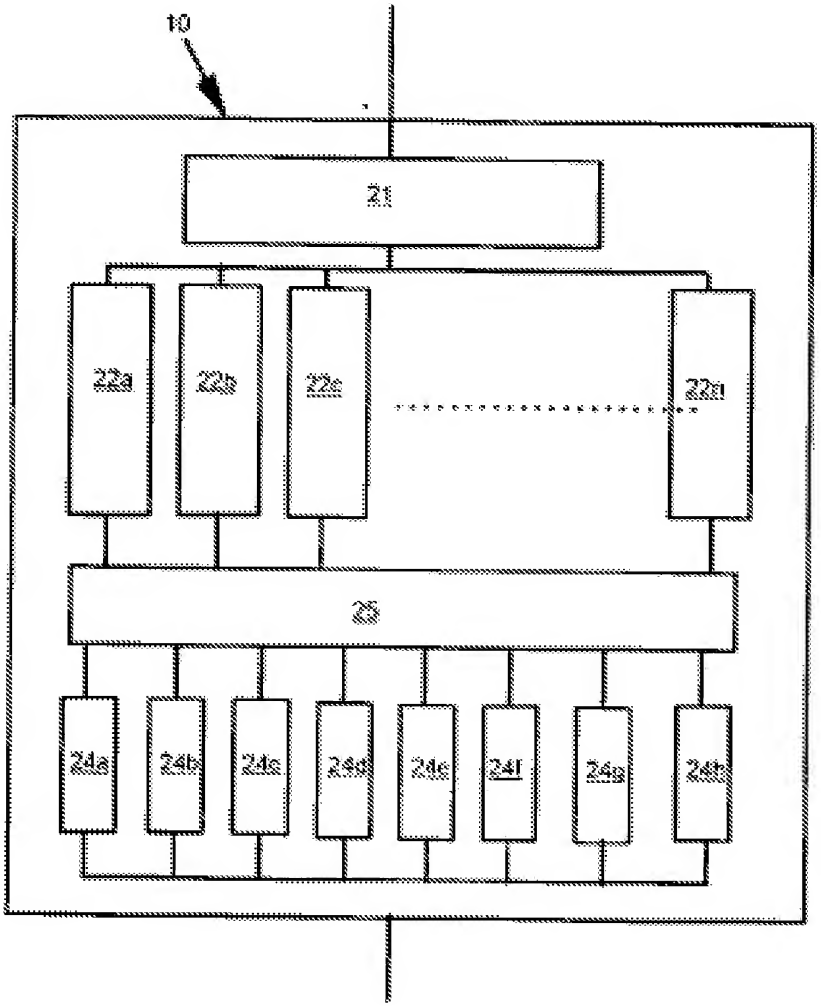


Fig. 2

EXHIBIT B

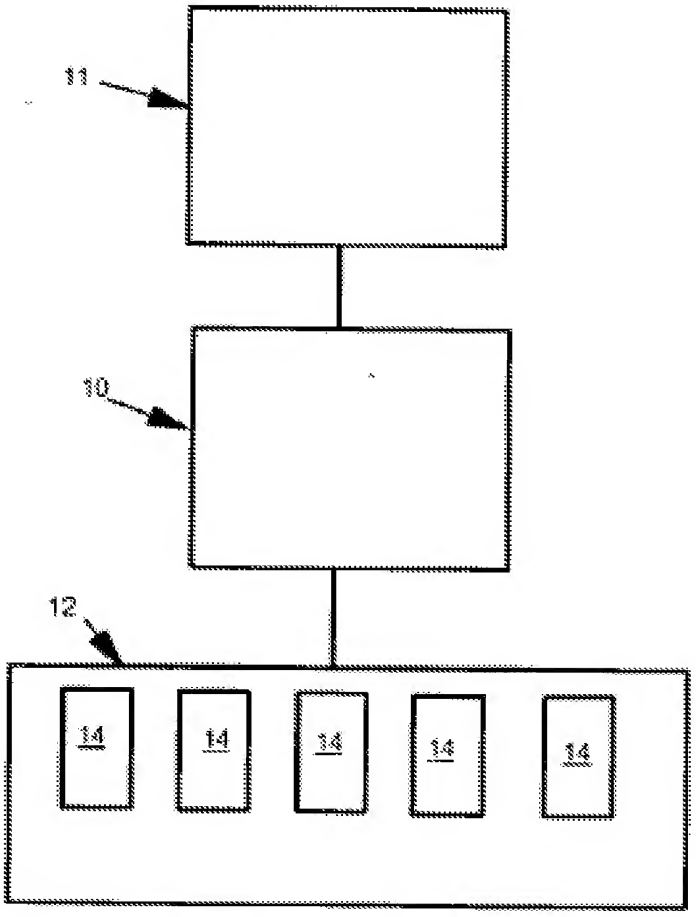


Fig. 1

EXHIBIT C

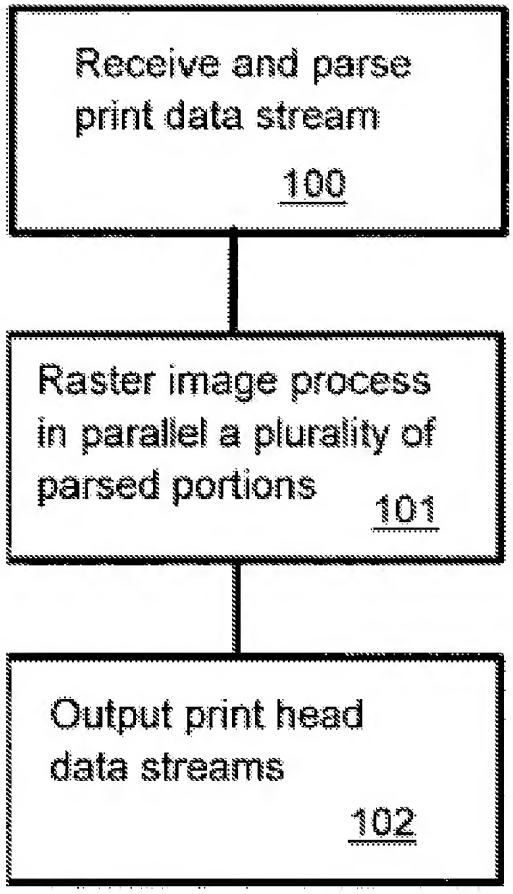


Fig. 3

EXHIBIT D

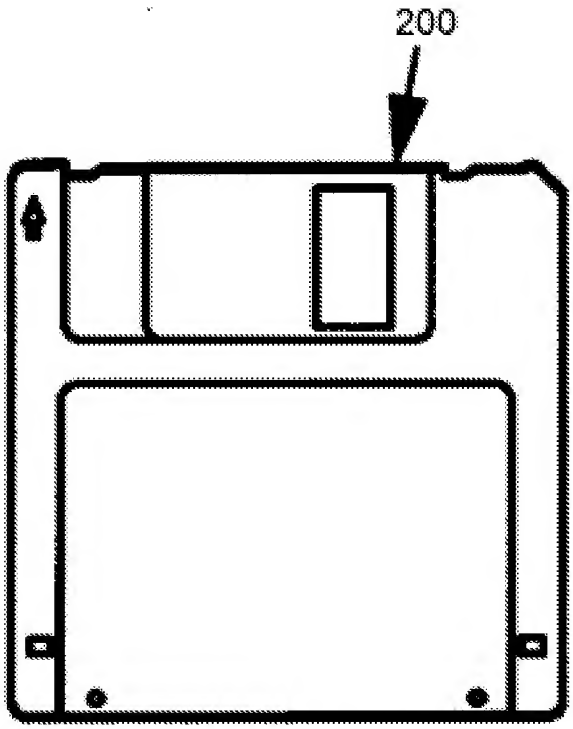


Fig. 4

EXHIBIT E

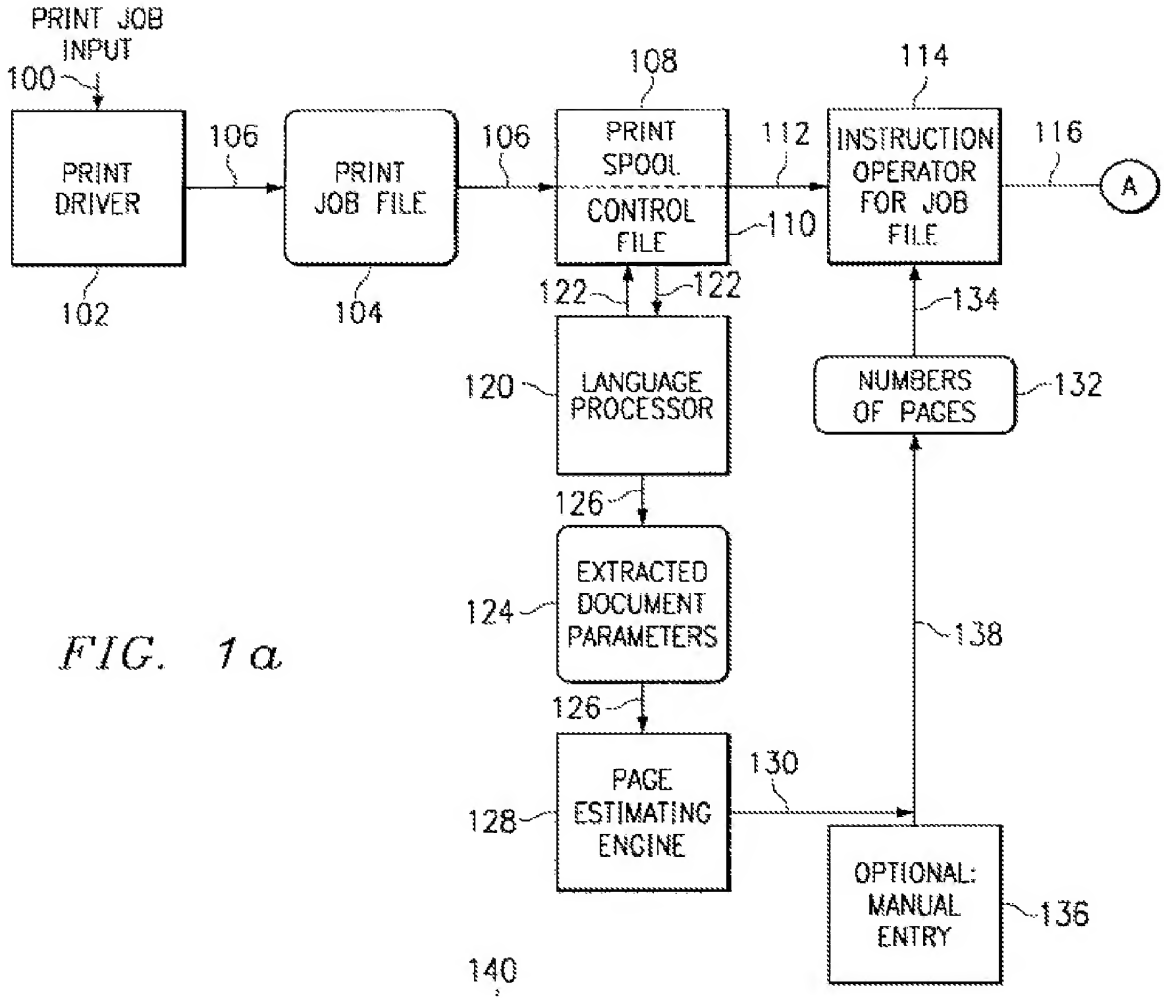


FIG. 1a

EXHIBIT F

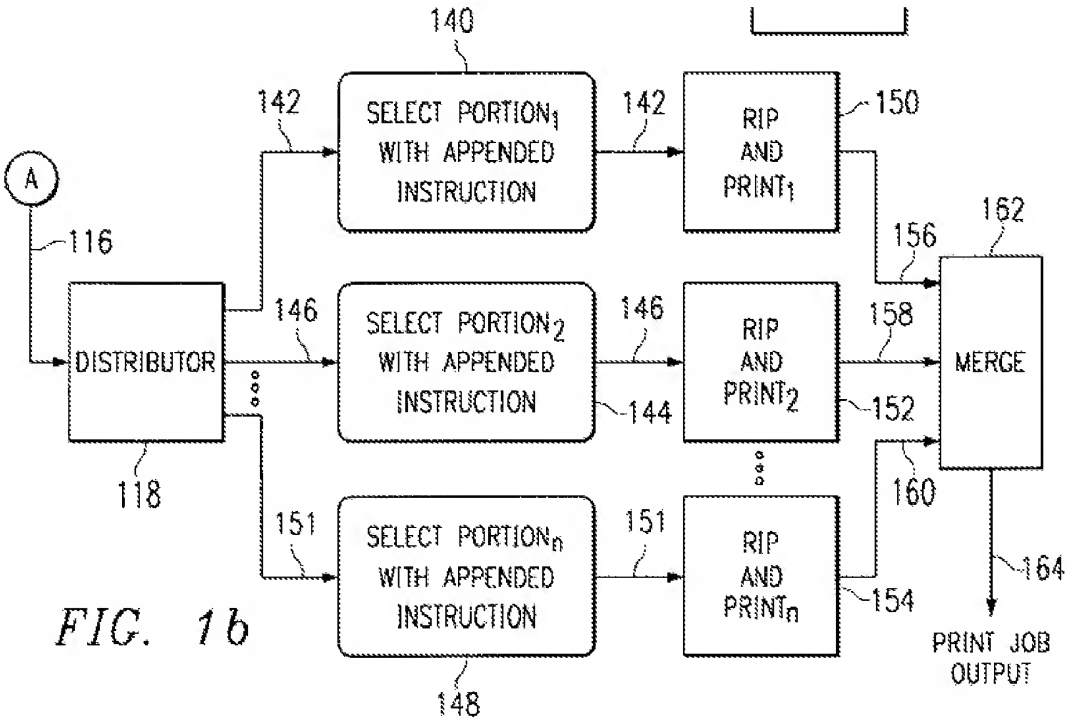


FIG. 1b

EXHIBIT G

FIG. 3

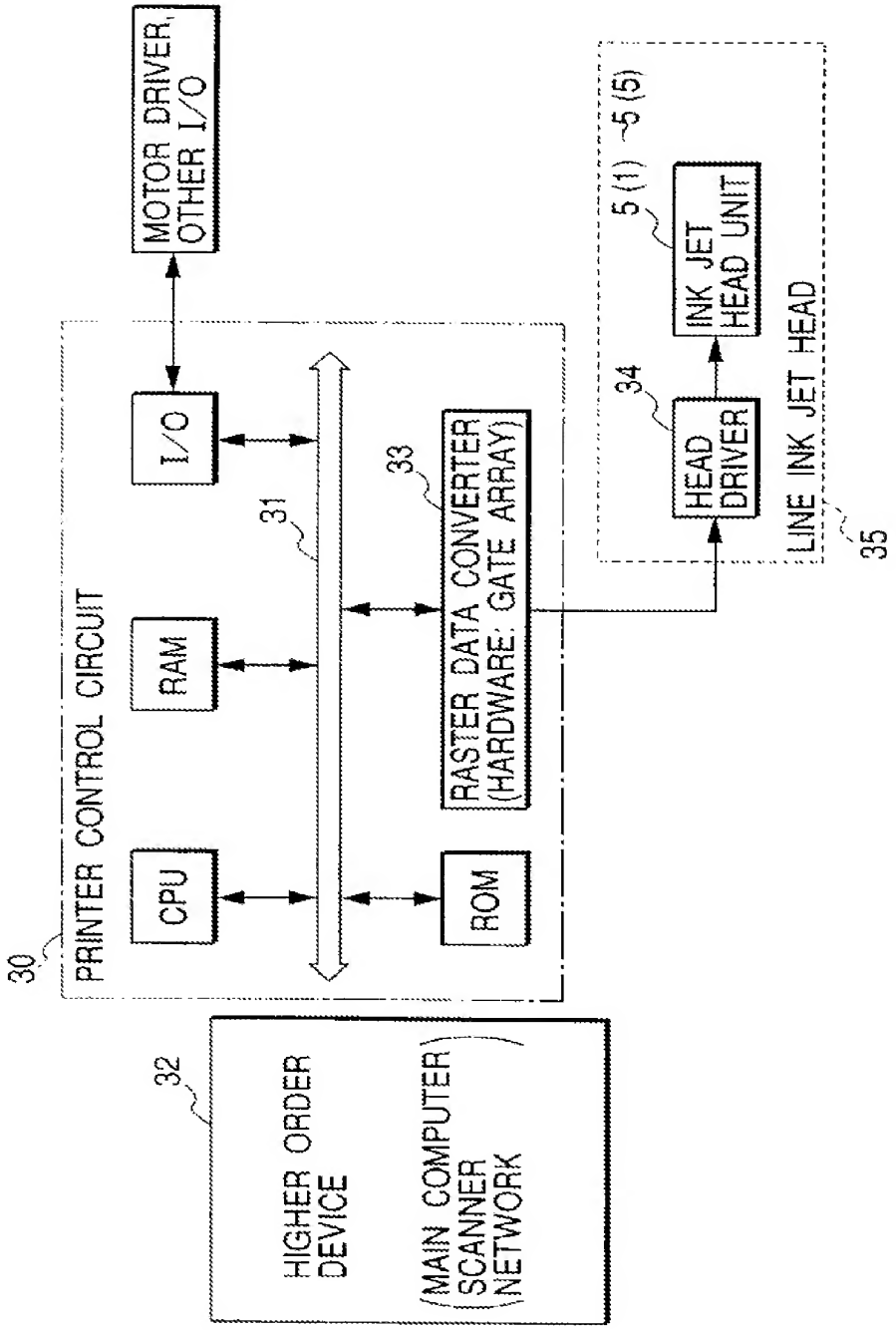


EXHIBIT H

FIG. 11

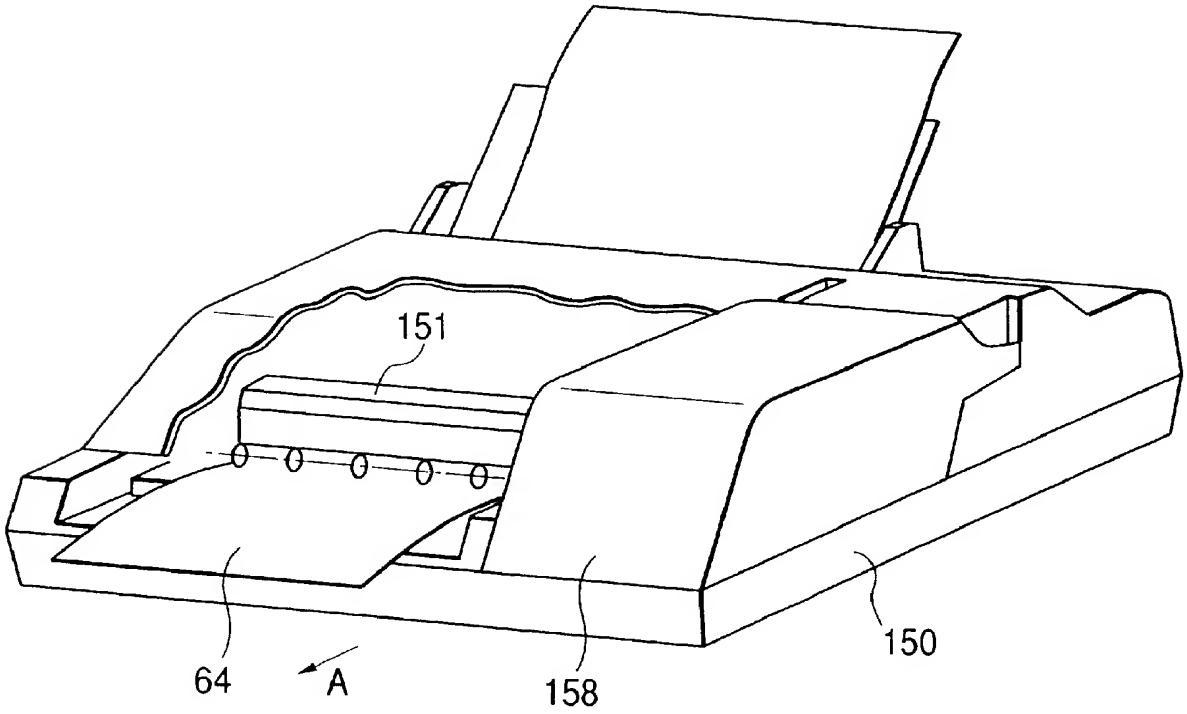


EXHIBIT I

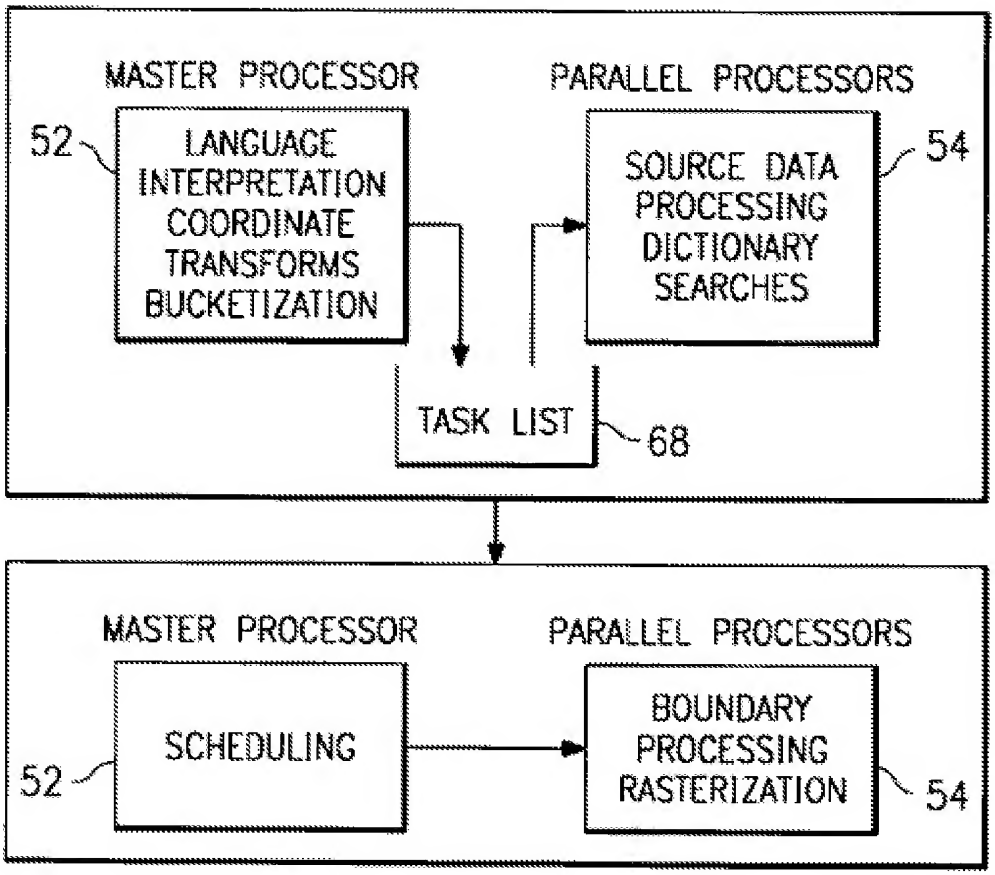
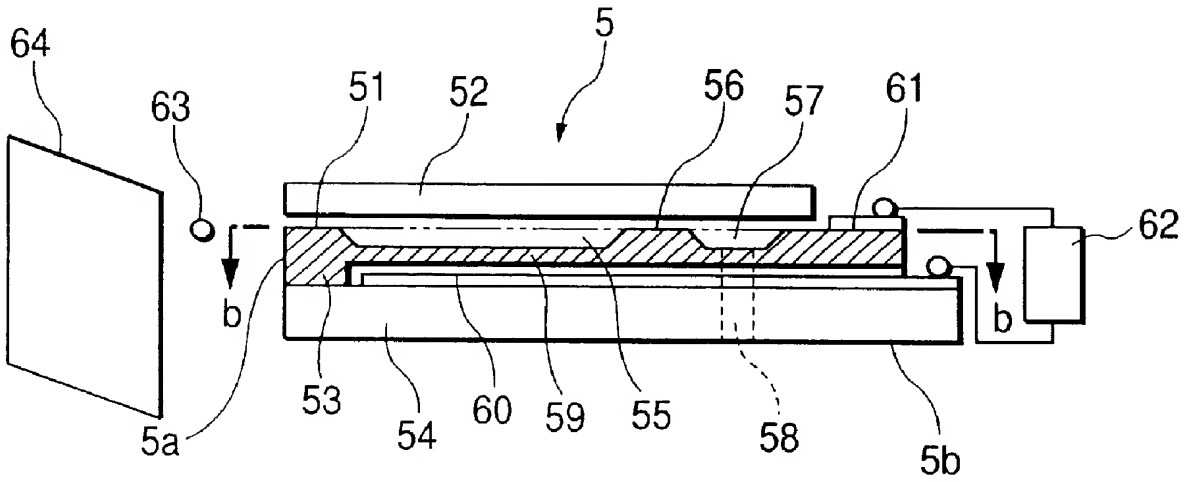

MASTER PROCESSOR
PARALLEL PROCESSORS
52
LANGUAGE
INTERPRETATION
COORDINATE
TRANSFORMS
BUCKETIZATION
SOURCE DATA
PROCESSING
DICTIONARY
SEARCHES
54
TASK LIST
68
MASTER PROCESSOR
PARALLEL PROCESSORS
SCHEDULING
52
BOUNDARY
PROCESSING
RASTERIZATION
54

EXHIBIT J

FIG. 2(a)



RELATED PROCEEDINGS APPENDIX

Pursuant to 35 U.S.C. §41.37(c)(x), copies of the following decisions rendered by a court of the Board in any proceeding identified above under 35 U.S.C. §41.37(c)(1)(ii) are enclosed herewith. As appellants are aware no decisions or proceedings having a bearing on the present appeal, nothing is included in the Appendix.